ECR #: 46
Title: Clarification of address alignment for Fast Write transactions
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Spec Version: A.G.P. 2.0

Summary:
A few questions about the address alignment of Fast Write transactions indicates a clarification in the description of Addressing Modes and Bus Operation and Fast Write Transfers is needed.

Change current text as follows: (changes underlined)

Section 3.2.2. Addressing Modes and Bus Operations, item 3

Memory addresses used in A.G.P. transactions, which are initiated by the AGP master, are always aligned on 8-byte boundaries; 8 bytes is the minimum access size, and all accesses are integer multiples of 8 bytes in length[1] (Memory accesses for PCI transactions have 4-byte granularity, aligned on 4-byte boundaries). A Fast Write transaction which is initiated by the corelogic is treated like a PCI transaction since it is initiated with **FRAME#** and not like an AGP transaction. Smaller or odd size reads must be accomplished with a PCI read transaction. Smaller or odd size writes may be accomplished via the **C/BE#** signals, which enable the actual writing of individual bytes within an eight byte field.

3.5.3.5. Fast Write Transfers

The Fast Write (FW) transaction is from the corelogic to the A.G.P. master acting as a PCI target. A FW transaction, regardless of the speed of the transaction (1x,2x,4x mode), always has 4-byte granularity and is aligned on a 4-byte boundary. This type of access is required to pass data/control directly to the A.G.P. master instead of placing the data into main memory and then having the A.G.P. master read the data. For 1x transactions, the protocol simply follows the PCI bus specification. However, for higher speed transactions (2x or 4x), FW transactions will follow a combination of PCI and A.G.P. bus protocols for data movement which is defined in this section. PCI protocol will be followed to initiate the transaction, while flow control will follow the A.G.P. block style and not PCI data phase style. Termination of the transaction is like PCI with some modifications to relationships between signals. For example, PCI requires **IRDY#** to be asserted when **FRAME#** is deasserted. However, for FW transactions, this relationship is not required.

[1] The motivation for increasing the addressing granularity from 4 bytes (PCI) to 8 bytes is tied to the typical memory organization used with 64-bit processors. Memories for these systems will generally be 64 bits wide. Therefore, smaller accesses will not provide any performance savings at the memory, and the motivation of A.G.P. is centered around maximizing memory performance for graphics accelerators.